# Outline

**HK9108 3Ω 7.3WF high withstand voltage type, monaural audio amplifier**

# characteristic

HK9108 is a 4Ω6W, mono AB / D audio power amplifier. HK9108 can easily switch to a class AB mode MODE pin, completely eliminate interference EMI. HK9108 operating voltage range of 2.5-7V. In the class D amplifier mode may provide greater than 90% efficiency, the new filter structure may be omitted without input low-pass filter of a conventional class D amplifier,

HK9108 uniqueof DRC( Dynamic range controlWhen) technology, reducing the power output due to waveform distortion caused toppers, compared to similar products, better dynamic response.

HK9108 using ESOP-8 package.

# application

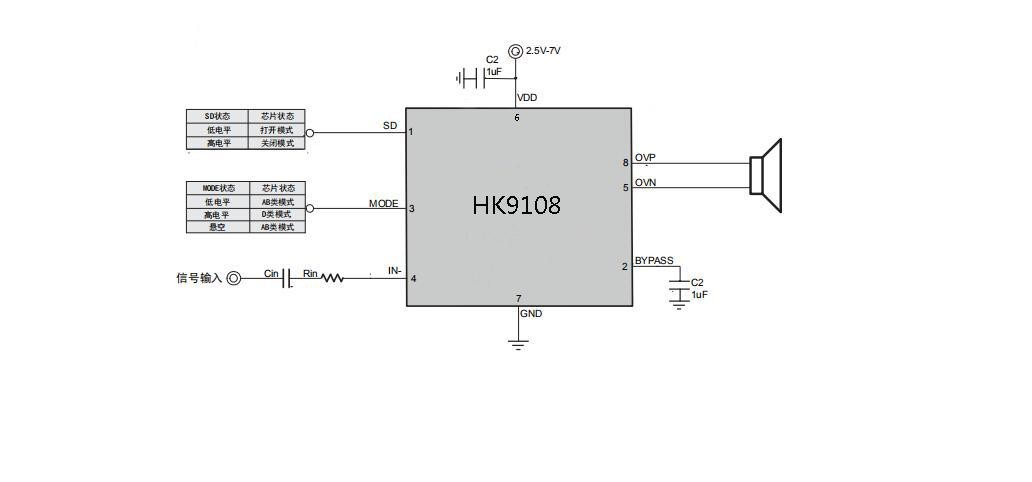
* Bluetooth speakers, intelligent speaker
* Navigation systems, portable game consoles,
* Children's toys, DVD, MP3, MP4
* Smart home and other audio products

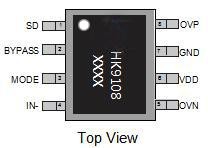
# Typical Application Diagram

* Input voltage range 2.5V-7V
* Filterless Class D / AB amplifier with low EMI and low quiescent current
* FM mode without interference
* Blow excellent suppression circuitry
* Ultra-low noise floor, low distortion
* 10% THD + N, VDD = 7V, 6W output power up to provide the load 4Ω + 33UH
* 10% THD + N, VDD = 7V, provides up to 7.3W output power under load 3Ω + 33UH
* Over-temperature protection, short circuit protection
* Shutdown Current <1ua

# Package

|  |  |  |
| --- | --- | --- |
| DH | Package Type | Package size |
| HK9108 | ESOP-8 |  |







Thermal Pad

ottom View

|  |  |  |  |
| --- | --- | --- | --- |
| **Pin Number** | **Pin Name** | **IO** | **Features** |
| 1 | SD | I | Shutdown control. High off, low open |
| 2 | BYPASS | IO | Internal common-mode reference voltage to the capacitor Shimoji |
| 3 | MODE | I | Mode switching. High in the D, low class AB floating default class AB |
| 4 | IN | I | An analog input terminal, an inverting |
| 5 | OVN | O | The negative output terminal |
| 6 | VDD | IO | Positive power supply terminal |
| 7 | GND | IO | Negative Power Supply |
| 8 | OVP | O | Output upright pole |

# The maximum limit

|  |  |  |  |
| --- | --- | --- | --- |
| **parameter name** | **symbol** | **Numerical** | **unit** |
| Supply voltage | VDD | 7V (MAX) | V |
| storage temperature | TSTG | -65 ℃ -150 ℃ | ℃ |
| Junction temperature | TJ | 160 ℃ | ℃ |
| Load  impedance | RL | ≧ 2 | Ω |

* **Recommended operating range**

|  |  |  |  |
| --- | --- | --- | --- |
| **parameter name** | **symbol** | **Numerical** | **unit** |
| Supply voltage | VDD | 3-6.5V | V |
| Working temperature | TSTG | 20 ℃ to 35 ℃ | ℃ |
| Junction temperature | TJ | - | ℃ |

**NOTES:**To ensure the safety and life of the chip, in strict accordance with recommended operating conditions for use in practical applications, otherwise, it may damage the chip.

# ESD information

|  |  |  |  |
| --- | --- | --- | --- |
| **parameter name** | **symbol** | **Numerical** | **unit** |
| Body static | HBM | ± 2000 | V |
| Electrostatic machine model | CDM | ± 300 | ℃ |

* **The basic electrical characteristics**

AV = 20dB, TA = 25 ℃, no special items are described in the VDD = 5V, 4Ω + 33uH under test conditions:

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| **description** | **symbol** | **Test Conditions** | | **Minimum** | **Typical values** | **Maximum** | **unit** |
| Quiescent Current | IDD | VDD = 5V, Class D | | 3 | 5 | 6 | mA |
| VDD = 4.2V, AB type | |  | 8 |  | mA |
| Off current | ISHDN | VDD = 3V to 5 V | | - | 1 |  | uA |
| Static noise floor | Vn | VDD = 5V, AV = 20DB, Awting | |  | 110 |  | uV |
| Frequency Class D | FSW | VDD = 5V | |  | 520 |  | kHz |
| Output offset voltage | Vos | VIN= 0V | |  | 10 |  | mV |
| Start Time | Tstart | Vdd = 5V, Bypass = 1uF | |  | 174 |  | MS |
| Gain | Av | Class D mode, RIN= 27k | |  | ≈20 |  | DB |
| Voltage power off | Vddsd | SD = 0 | |  | <1.6 |  | V |
| Power turn-on voltage | Vddopen | SD = 0 | |  | > 2.5 |  | V |
| SD-off voltage | Vsdsd | Vdd = 7V | |  | > 1.8 |  | V |
| - | |  |  |  |
| Vdd = 5V | |  | > 1.6 |  |
| Vdd = 4V | |  | > 1.4 |  |
| Vdd = 3V | |  | > 1.4 |  |
| SD threshold voltage | Vsdopen | Vdd = 7V | |  | <1.0 |  | V |
| - | |  |  |  |
| Vdd = 5V | |  | <0.9 |  |
| Vdd = 4V | |  | <0.8 |  |
| Vdd = 3V | |  | <0.7 |  |
| Class D on voltage | MODE/ D | Vdd = 7V | |  | > 2.0 |  | V |
| - | |  |  |  |
| Vdd = 5V | |  | > 1.8 |  |
| Vdd = 4V | |  | > 1.6 |  |
| Vdd = 3V | |  | > 1.4 |  |
| AB class turn-on voltage | MODE/ AB | Vdd = 7V | |  | <1.4 |  | V |
| - | |  |  |  |
| Vdd = 5V | |  | <1.2 |  |
| Vdd = 4V | |  | <1.0 |  |
| Vdd = 3V | |  | <0.8 |  |
| Over-temperature protection | OTP |  | |  | 180 |  | ℃ |
| Static on-resistance | RDSON | IDS= 0.5AVGS= 4.2V | P\_MOSFET |  | 150 |  | mΩ |
| N\_MOSFET |  | 120 |  |
| Built input resistor | Rs |  | |  | 7K |  | KΩ |
| Built-in feedback resistor | Rf |  | |  | 180K |  | KΩ |
| effectiveness | ηC |  | |  | 90 |  | % |

### Class\_D power

AV = 20dB, TA = 25 ℃, no special instructions are items at VDD = 5V, 4Ω Test conditions:

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| **parameter** | **symbol** | **Test Conditions** | | **Minimum** | **Typical values** | **Maximum** | **unit** |
| Output Power | Po | THD + N = 10%,  f = 1kHz, RL= 3Ω; | VDD= 7V | - | 7.3 | - | W |
| VDD= 6V | - | 5.3 | - |
| VDD= 5V |  | 3.7 |  |
| VDD= 4.2V |  | 2.6 |  |
| THD + N = 10%,  f = 1kHz, RL= 4Ω | VDD= 7V |  | 6 |  |
| VDD= 6V |  | 4.5 |  |
| VDD= 5V |  | 3.1 |  |
| VDD= 4.2V |  | 2.2 |  |
| Total harmonic distortion plus noise | THD + N | VDD= 5VPo= 1W, RL= 4Ω | f = 1kHz | - | 0.065 | - | % |

# Performance characteristic

### Characteristic Test Conditions (TA = 25 ℃)

|  |  |  |
| --- | --- | --- |
| **description** | **Test Conditions** | **Numbering** |
| Input Amplitude VS. Output Amplitude | VDD = 5V, RL = 4Ω + 33UH, Class\_D | figure 1 |
| Output Power VS. THD + N \_Class\_D | RL = 3Ω + 33UH, AV= 20DB, Class\_D | figure 2 |
| RL = 4Ω + 33UH, AV= 20DB, Class\_D | image 3 |
| Output Power VS.THD + N\_Class\_AB | RL = 4Ω, AV= 20DB, Class\_AB | Figure 4 |
| Frequency VS.THD + N | VDD = 5V, RL = 4 Ω, AV= 20DB, PO = 1W, Class\_D | Figure 5 |
| Input Voltage VS.Power Crrent | VDD = 3.0V-5V, Class\_D | Figure 6 |
| Input Voltage VS. Maximum Output Power | RL = 4Ω + 33UH, THD = 10%, Class\_D | Figure 7 |
| Frequency Response | VDD = 5V, RL = 4Ω, Class\_D | Figure 8 |

FIG 1: Input Amplitude VS. Output Amplitude FIG 2: THD + N VS .Output Power Class\_D



D

D =

V RL = 4Ω + 33

uH

Cla

ss

10000

Input Amplitude VS Output Amplitude

1000

100

10

V5

\_D

10

100

1000

10000

Input Amplitude (mVrms)



100

VDD = 7V RL = 3Ω + 22uH Class\_D

THD + N VS Output Power

10

VDD = 6V RL = 3Ω + 22uH Class\_D

VDD = 5V RL = 3Ω + 22uH Class\_D VDD = 4.2V RL = 3Ω + 22uH Class\_D

1

0.1

0.01

0.1

1

Output Power (W)

10

Output Amplitude (mVrms)

THD + N (%)

FIG 3: THD + N VS .Output Power Class\_D FIG 4: THD + N VS. Output Power Class\_AB



100

10

THD + N VS Output Power

VDD = 7V RL = 4Ω + 33uH Class\_D VDD = 6V RL = 4Ω + 33uH Class\_D VDD = 5V RL = 4Ω + 33uH Class\_D VDD = 4.2V RL = 4Ω + 33uH Class\_D

1

0.1

0.01

0.1

1

Output Power (W)

10



Output Power VS THD + N%

100

VDD = 5V RL = 4Ω Claas\_AB

VDD = 4.2V RL = 4Ω Claas\_AB

10

1

0.1

0.01

0.1

1

Output Power (W)

10



10

Frequency VS THD + N%

VDD = 5V PO = 1W RL = 4Ω + 33uH

1

0.1

0.01

0.001

10

100

1000

10000

Frequency (HZ)

7

Input Voltage VS Power Current

6

5

4

3

2

1

33.544.555.566.57

Input Voltage (V)

THD + N%

THD + N%

Power Current (ma)

THD + N (%)

Figure 5: Frequency VS.THD + N Figure 6:Power Crrent VS. Suppy Voltage

7

Input Voltage VS Power Current

6

5

4

3

2

1

33.544.555.566.57

Input Voltage (V)



V

DD

=

RL =

4Ω Cla

ss\_

D

3

2

1

0

-1

-2

-3

-4

-5

-6

Frequency Response

5V

10

100

1000

10000

Frequency (HZ)

Power Current (ma)

Gain (db)

**Figure 7:**Input Voltage VS. Maximum Output Power Figure 8:Frequency Response

# Application Note

### SD pin control

SD pin is a chip enable pin. Controlling opening and closing of the chip,

SD pin is high, the power amplifier chip off. SD pin isLow, the amplifier chip open, normal operation. SD pin can not be suspended.

|  |  |
| --- | --- |
| SD pin | Chip Status |
| Low | Open state |
| High | Disabled |

### MODE pin control

MODE pin can control the mode amplifier chip class AB and class-D switching. We recommend switching to class AB in the FM mode.

|  |  |
| --- | --- |
| MODE pin | Chip Status |
| High | Class D mode |
| Low | Class AB mode |
| Suspended | Class AB mode |

### Amplifier gain control

Output (PWM signal) based upon the digital signal D mode, AB class outputAn analog signal, which can gain by RIN adjusted.

180*K*

### Bypass capacitance

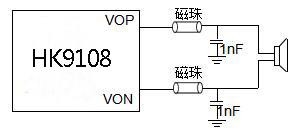
Byp capacitance is very important, the size of the capacitor determines the powerOpening the discharge time of the chip, while the chip size affects Byp important properties capacitance power supply rejection ratio, noise, sound, etc., and POP.

The capacitance was set to recommend 1uf, because of the charge rate Byp

Slower than the charging speed of the input signal terminal, POP sound smaller.

### EMI deal

Take longer for the output line or near sensitive devices, it proposes to addMagnetic beads and capacitor, can effectively reduce EMI. Placed close to the chip device.



### RC snubber

The loudspeaker load impedance value is small, and at the output a recommendedResistor and a capacitor to absorb voltage spikes, to prevent abnormal working chip.

## *A*  2 

*V RIN*  7*K*

Recommended resistance: 2Ω-5Ω, capacitance recommended: 500PF-10NF.

AV is the gain, usually expressed DB, multiple units of the above-described calculation result, multiple 20Log = DB.

Unit resistor RIN is KΩ, 180KΩ feedback resistor to the internal

(RF), 7KΩ series resistor is built (RS), RIN based on the actual supply voltage, the input amplitude, distortion, and defined by the user. Such as RIN = 27K, = 10.5 times, AV = 20.4DB

Input capacitor (CIN) and input resistor (RIN) composed of a high-pass filterFilter, whose cutoff frequency is:

*fC* 



* 7*K*

1



2** *R* 

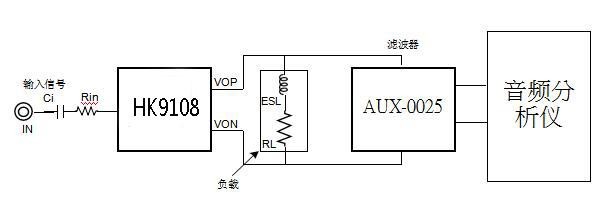
*IN*

*CIN*

Selecting a smaller value when the capacitance Cin, can be filtered from an input terminal coupledThe low-frequency noise, while helping to reduce the noise generated when opening POPO

# Test Methods

The filter must be added when testing the class D mode. AUX-0025 is a filter. To test the accuracy of the data and realistic applications, RLA load end of the series inductor, analog parasitic inductance of the speaker.



# PCB Design Considerations

* Power supply pin (VDD) if traces via a network connection must be porous, and an inner diameter vias increase, not a single viasdirect connection.
* Input capacitance (Cin), the input resistance (Rin of) pins are placed as close to the power amplifier chip, the package is preferably used to trace mode, there may beThe effect of suppressing noise other signal coupling.
* HK9108 bottom fins welded recommendations PCB board for chip cooling, it is recommended to use a large copper PCB is connected to the intermediate chip fins, and have a range of exposed copper, help chip cooling.
* HK9108 is connected to the speaker output pin alignment pins as short as possible, and the required track width 0.4mm or more.

# Chip Package ESOP-8

C2

e

D

C3



A

b

C

C1

L

B

D1

L θ2



E3

θ1

**ESOP-8**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **character** | **Dimensions In Millimeters** | | | **Dimensions In Inches** | | |
| **Min** | **Nom** | **Max** | **Min** | **Nom** | **Max** |
| **A** | 2.31 | 2.40 | 2.51 | 0.091 | 0.094 | 0.098 |
| **B** | 3.20 | 3.30 | 3.40 | 0.126 | 0.129 | 0.132 |
| **b** | 0.33 | 0.42 | 0.51 | 0.013 | 0.017 | 0.020 |
| **C** | 3.8 | 3.90 | 4.00 | 0.150 | 0.154 | 0.157 |
| **C1** | 5.8 | 6.00 | 6.2 | 0.228 | 0.235 | 0.244 |
| **C2** | 1.35 | 1.45 | 1.55 | 0.053 | 0.058 | 0.061 |
| **C3** | 0.05 | 0.12 | 0.15 | 0.004 | 0.007 | 0.010 |
| **D** | 4.70 | 5.00 | 5.1 | 0.185 | 0.190 | 0.200 |
| **D1** | 1.35 | 1.60 | 1.75 | 0.053 | 0.06 | 0.069 |
| **e** | 1.270 (BSC) | | | 0.050 (BSC) | | |
| **L** | 0.400 | 0.83 | 1.27 | 0.016 | 0.035 | 0.050 |